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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,790	01/21/2004	Albert E. Cosand	PD-03W012	3552

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,790	COSAND, ALBERT E.	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *56-61, 63, 65, 67-68, 70, 72, 74-75, 77 and 79-83* is/are allowed.

6)☒ Claim(s) *1-55, 66, 73 and 84* is/are rejected.

7)☒ Claim(s) *62, 64, 69, 71, 76, and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/21/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. An initiated copy of the information disclosure statement (IDS) submitted on 01/21/2005 is attached herewith.

Specification

2. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Claim Objections

3. Claims 2-3 are objected to because of the phrases: "said first set of complementary output signals" and "said second set of complementary output signals" are unclear. Clarification/correction is required.

4. Claims 6, 8, 13, 15, 20, 22, 34, 36, 41, 43, 48, 50, 62, 64, 69, 71, 76, and 78 are unclear because of "NPN" and "PNP" are not specified. Clarification is required.

5. Claims 25 & 53 is objected because of "the **first** and sixth transistors..." Should it read as "the **fifth** and sixth transistors...?" Correction or clarification is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 10, 17, 38, 45, 66, 73, and 84 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, "the second set of complementary signals for..." lacks antecedent basis. Correction is required.

Regarding claims 10, 38, and 66, "the first intermediate signal" and "the second intermediate signal" lack antecedent basis. Clarification or correction is required.

Regarding claims 17, 45, and 73, "the third intermediate signal" and "the fourth intermediate signal" lack antecedent basis. Clarification or correction is required.

Regarding claim 84, "the first set of signals" and "the second set of signals" lack antecedent basis. Clarification or correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-55 and 84 are rejected under 35 U.S.C. 102(b) as being anticipated by Metz et al. (US 4,663,610).

Regarding claim 1, Metz et al. discloses a switching circuit (Figs. 1-2) comprising:

first means (including FF1 and transistors Q1/Q2) responsive to a first set of complementary signals (signals output from Q/Q-bar terminals of flip-flop FF1, 30) for providing complementary output signals (at collectors of transistors Q1/Q2);

second means (including FF2 and transistors Q3/Q4) responsive to a second set of complementary signals (signals output from Q/Q-bar terminals of flip-flop FF2, 32) for providing complementary output signals (at collectors of transistors Q3/Q4); and

third means (including transistors Q5/Q6) for selectively activating the first means or the second means in response to a control signal (the control signals CLK2 or CLK2-bar provided from the control circuit 38).

Regarding claim 2, Metz et al. discloses the complementary output signals, which provided by the first means in claim 1 is provided by a master latch (first flip flop FF1 of Fig. 1 and/or Fig. 2).

Regarding claim 3, Metz et al. discloses the complementary output signals, which provided by the second means in claim 1 is provided by a slave latch (second flip flop FF2 of Fig. 1 and/or Fig. 2).

Regarding claim 4, Metz et al. discloses the first means of claim 1 includes a first differential pair of transistors (Q1, Q2).

Regarding claim 5, Metz et al. discloses the first differential pair of transistors of claim 4 includes first and second transistors Q1 and Q2, respectively (see, Fig. 2).

Regarding claims 6-9, Metz et al. discloses the first and second transistors of claims 5 are field effect transistors (PNP or NPN Q1/Q2) and connected in a common emitter configuration (emitters of Q1/Q2 are connected).

Regarding claim 10, Metz et al. discloses the invention of claim 5 wherein a first intermediate signal (output signal provided from the Q terminal of FF1 – Figs. 1-2) is provided as an input to the first transistor (Q1) and a second intermediate signal (output signal provided from the Q-bar terminal of FF1 – Figs. 1-2) is provided as an input to the second transistor (Q2).

Regarding claim 11, Metz et al. discloses the invention of claim 5 wherein the second means includes a second differential pair of transistors (Q3/Q4 – Fig. 2).

Regarding claim 12, Metz et al. discloses the invention of claim 11 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively (Q3/Q4 of Fig. 2).

Regarding claims 13-16, Metz et al. discloses the third and fourth transistors of the above claims are field effect transistors (PNP or NPN Q3/Q4) and connected in a common emitter configuration (emitters of Q3/Q4 are connected).

Regarding claim 17, Metz et al. discloses the invention of claim 12 wherein a third intermediate signal (output signal provided from the Q terminal of FF2 – Fig. 2) is provided as an input to the third transistor (Q3) and a fourth intermediate signal (output signal provided from the Q-bar terminal of FF2 – Fig. 2) is provided as an input to the fourth transistor (Q4).

Regarding claims 18-23, Metz et al. discloses the invention of claim 11 wherein the third means includes a third differential pair of field effect transistors (fifth and sixth PNP or NPN transistors Q5-Q6) and connected in a common emitter configuration (emitters of Q5/Q6 are connected).

Regarding claim 24, Metz et al. discloses the invention of claim 19 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals (CLK2 and CLK2-bar).

Regarding claims 25-27, Metz et al. discloses the invention of claim 24 wherein the fifth [first] and sixth transistors (Q5/Q6) have a terminal (emitter terminals)

connected to a source (cascade current source 50) and a terminal connected to one of the first differential pair (Q1/Q2) and the second differential pair (Q3/Q4).

Regarding claim 28, Metz et al. discloses a switch circuit (Figs. 1-2) comprising:

first means (FF1) for providing a first set of first and second complementary intermediate signals (Q and Q-bar signal pair);

second means (FF2) for providing a second set of third and fourth complementary intermediate signals (Q and Q-bar signal pair);

third means (including Q1/Q2 pair) responsive to the first set of signals for providing complementary output signals (from FF1);

fourth means (including Q3/Q4 pair) responsive to the second set of signals for providing complementary output signals (from FF2); and

fifth means (including Q5/Q6) for selectively activating the third means or the fourth means in response to a control signal (CLK2 and CLK2-bar).

Regarding claims 29-30, Metz et al. discloses the invention of claim 28 wherein the first means is a master latch (first latch means FF1) and the second means is a slave latch (second latch means FF2).

Regarding claims 31, Metz et al. discloses (see Fig. 1) the invention of claim 30 wherein the slave latch (second latch FF2, 14) has inputs provided by the master latch (first latch FF1, 10).

Regarding claims 32-37, Metz et al. discloses the invention of claim 28 wherein the third means includes a first differential pair of field effect transistors (first and second PNP or NPN transistors Q1-Q2) and connected in a common emitter configuration (emitters of Q1/Q2 are connected).

Regarding claim 38, Metz et al. discloses the invention of claim 33 wherein a first intermediate signal (output signal provided from the Q terminal of FF1 – Figs. 1-2) is provided as an input to the first transistor (Q1) and a second intermediate signal (output signal provided from the Q-bar terminal of FF1 – Figs. 1-2) is provided as an input to the second transistor (Q2).

Regarding claims 39-44, Metz et al. discloses the invention of claim 33 wherein the fourth means includes a second differential pair of field effect transistors (third and fourth PNP or NPN transistors Q3-Q4) and connected in a common emitter configuration (emitters of Q3/Q4 are connected).

Regarding claim 45, Metz et al. discloses the invention of claim 40 wherein a third intermediate signal (output signal provided from the Q terminal of FF2 – Fig. 2) is provided as an input to the third transistor (Q3) and a fourth intermediate signal (output signal provided from the Q-bar terminal of FF2 – Fig. 2) is provided as an input to the fourth transistor (Q4).

Regarding claims 46-51, Metz et al. discloses the invention of claim 39 wherein the fifth means includes a third differential pair of field effect transistors (fifth and sixth PNP or NPN transistors Q5-Q6) and connected in a common emitter configuration (emitters of Q5/Q6 are connected).

Regarding claim 52, Metz et al. discloses the invention of claim 47 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals (CLK2 and CLK2-bar).

Regarding claims 53-55, Metz et al. discloses the invention of claim 52 wherein the fifth [first] and sixth transistors (Q5/Q6) have a terminal (emitter terminals) connected to a source (cascade current source 50) and a terminal connected to one of the first differential pair (Q1/Q2) and the second differential pair (Q3/Q4).

Regarding claim 84, Metz et al. discloses a method of switching associated with the apparatus of rejected claim 1 (Figs. 1-2) comprising the steps of:

providing (by first latch FF1) a first set of first and second complementary intermediate signals (signals outputted from Q and Q-bar terminals of FF1);

providing (by second latch FF2) a second set of third and fourth complementary intermediate signals (signals outputted from Q and Q-bar terminals of FF2);

providing (by switching differential pair Q1/Q2) a first set of complementary output signals (output of differential pair Q1/Q2) in response to the first set of signals (signals outputted from the Q and Q-bar terminals of FF1);

providing (by switching differential pair Q3/Q4) a second set of complementary output signals (output of differential pair Q3/Q4) in response to the second set of signals (signals outputted from the Q and Q-bar terminals of FF2); and

selecting (by steering the transistor pair Q5/Q6) the first or the second set of complementary output signals in response to a control signal (by the selection/steering signals CLK2 and CLK2-bar).

8. Claims 62, 64, 66, 69, 71, 73, 76, and 78, are objected/rejected for the reasons indicated above. Claims 56-61, 63, 65, 67-68, 70, 72, 74-75, 77, and 79-83 are allowed.

Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclose: US 5,597,303; US 6,628,220; US 6,888,485; US 6,778,116; US 4,733,218; and US 6,061,010.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 3, 2005

Khai M. Nguyen
Art Unit: 2819
571-272-1809